

High-power high-efficiency 2D VCSEL arrays

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ABSTRACT

We review recent results on high-power, high-efficiency two-dimensional vertical-cavity surface-emitting laser (VCSEL) arrays emitting around 980nm. Selectively oxidized, bottom-emitting single VCSEL emitters with 51% power conversion efficiency were developed as the basic building block of these arrays. More than 230W of continuous-wave (CW) power is demonstrated from a ~5mm x 5mm array chip. In quasi-CW mode, smaller array chips exhibit 100W output power, corresponding to more than 3.5kW/cm² of power density. High-brightness arrays have also been developed for pumping fiber lasers, delivering a fiber output power of 40W. We show that many of the advantages of low-power single VCSEL devices such as reliability, wavelength stability, low-divergence circular beam, and low-cost manufacturing are preserved for these high-power arrays. VCSELs thus offer an attractive alternative to the dominant edge-emitter technology for many applications requiring compact high-power laser sources.

Keywords: Semiconductor lasers, vertical-cavity surface-emitting lasers (VCSELs), high efficiency, high-power, 2D array, pumping, solid-state laser, brightness, reliability.

1. INTRODUCTION

Historically, vertical-cavity surface-emitting lasers (VCSELs) have been mostly confined to low-power applications (a few mW at most), such as high-speed data transmission^{1,2}. However, there are no fundamental reasons why the VCSEL technology cannot be extended to very high-power applications by fabricating large two-dimensional (2D) arrays of low-power single-emitters. There are a few studies on VCSELs aimed at the increase of the output power of single devices and arrays. Devices operating around 100mW were first reported in³. Improvements in the epitaxial growth, processing, device design, and packaging led to VCSELs emitting several hundreds of milliwatts from single devices with very large apertures and from arrays⁴. More than 2W CW at -1°C heat-sink temperature was reported from a VCSEL array consisting of 1000 single elements⁵ corresponding to a power density of 30 W/cm². In another work⁶, more than 1W CW power and 10W pulsed (15ns) power was obtained at room temperature from a 19-element array. The 1W CW power corresponded to a 1kW/cm² power density. Finally, a record 3W CW output power has been reported from large (350µm-diameter aperture) single devices emitting around 976nm⁷.

Our idea is to extend to high power VCSELs most if not all the advantages that made the low-power VCSELs successful. Such advantages include low-cost manufacturing⁸, reliability⁹, spectral and beam quality. These advantages would make for an attractive high-power laser source in a wide variety of medical, industrial, and military applications such as: pumping of fiber and solid-state lasers, skin-care and hair-removal devices, printing, and projection displays (using frequency doubling), to name a few.

However, to compete with the existing edge-emitting laser technology in most applications, VCSELs need to improve their power conversion efficiency (PCE) beyond 50%. For high-power systems, the cost, size and weight are dominated by the input power supplies and refrigeration units, so high-efficiency is needed for the laser sources. The edge-emitter technology currently exceeds 70% power conversion efficiency¹⁰. However, unlike edge-emitters, VCSELs do not suffer from catastrophic optical damage (COD)¹¹, which means VCSELs can be operated reliably at high temperatures¹². In this case, the refrigeration unit can be altogether eliminated, which translates into a significant gain in overall system-level conversion efficiency, even if the VCSEL source itself has a lower conversion-efficiency than the edge-emitter source operating with a refrigeration unit¹³.

Top-emitting VCSEL devices exceeding 50% power conversion efficiency have already been demonstrated¹⁴. However, for high-power arrays, junction-down, bottom-emitting devices are required for efficient heat-removal⁶.

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The technical challenges for the development of a high-power VCSEL array can be summarized as follows: 1) Develop a high-efficiency bottom-emitting single-device; 2) Improve the growth and process uniformity for cm-scale chips; 3) Improve the packaging for reliability and kW-level heat-removal.

This paper first reviews the development effort of high-efficiency bottom-emitting VCSEL devices emitting around 976nm, leading to >50% power conversion efficiencies (PCE) over a wide range of aperture sizes. Then, the fabrication and packaging of large VCSEL arrays is discussed and results on the array are presented. For proper design of the array, we show that the PCE is preserved, with minimal drop compared to the single device results. Record CW output power >230W and QCW output power densities >3.5kW/cm² from large VCSEL arrays are demonstrated and we also show that the spectral and beam properties are preserved at the array level. Finally, results for high-brightness high-power arrays are presented.

2. DEVELOPMENT OF HIGH-EFFICIENCY VCSEL DEVICES

2.1 Device structure & fabrication

For high-power operation, efficient heat-removal is required and therefore a junction-down, bottom-emitting structure is preferred to improve current injection uniformity in the active region and to reduce the thermal impedance between the active region and the heat-spreader^{4,15}. A schematic of the structure without the heat-spreader is shown in Figure 1.

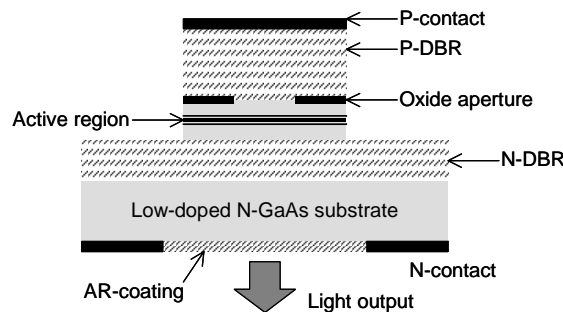


Fig. 1. Schematic of the selectively oxidized, bottom-emitting 976nm VCSEL structure.

For current and optical confinement, the selective oxidation process¹⁶ is used to create an aperture near the active region to improve performance¹⁷. A low-doped GaAs N-type substrate is used to minimize absorption of the output light while providing electrical conductivity for the substrate-side N-contact. The growth is performed in a MOCVD reactor and starts with an AlGaAs N-type distributed Bragg reflector (DBR), which in this case acts as the output coupler. The reflectivity of the N-DBR is optimized for maximum PCE¹⁸. The active region consists of InGaAs quantum wells designed for 976nm emission, and is followed by a high-reflecting P-type DBR. A high-Aluminum content layer is placed near the first pair of the P-DBR to later form the oxide aperture. The placement and design of the aperture is critical to minimize optical losses^{19,20} and current spreading²¹. Band-gap engineering (including modulation doping) is used to design low-resistivity DBRs with low-absorption losses²².

The processing of bottom-emitting single devices is straightforward. On the epitaxial side, Ti/Pt/Au disks of different diameters are evaporated to form the P-type contacts, which at the same time act as the self-aligned mask for subsequent dry-etching (RIE) of mesas, deep enough to expose the Aluminum-rich layer. The samples are then exposed to high humidity in a furnace (390~420°C) for the selective oxidation process. On the substrate side, the substrate is thinned to less than 150micron thickness to minimize absorption losses and then polished to an optical finish. A Si₃N₄ anti-reflection coating is deposited using PECVD, followed by patterning, etching of the field nitride and finally Ge/Au/Ni/Au N-metals evaporation. Finally, the devices are cleaved and packaged on heat-spreader submounts for testing.

2.2 Results and discussion

Individual devices are tested on a probe-station using a calibrated integrating-sphere/detector/power-meter system (Newport), a calibrated high-precision current source (ILX), and a calibrated voltmeter (Agilent). A TEC-controlled

stage maintains a constant heat-sink temperature. A four-point-probe measurement was used to record the voltage accurately. For accurate determination of the device PCE, precise calibration of the instruments is critical. For example, for devices with small threshold currents (<1mA), a small offset in the current source could result in a significant error in PCE for these devices. We continually cross-check our results using different sets of instruments. Also, as a participant of the DARPA Super-High Efficiency Diode Source (SHEDS) program we were able to calibrate our instruments against NIST's own results on our devices. As a result, we were able to improve the measurement error of our test set-up to better than +/-1%.

Figure 2 shows the L-I-V characteristics of a 16µm-diameter device at room temperature. Threshold current, differential slope efficiency, and differential resistance are 1mA, 77.5%, and 47.5Ω, respectively. A maximum PCE of 51.2% is achieved at 6.6mA (5.7mW). To the best of our knowledge, this is the highest PCE to date for a bottom-emitting 976nm VCSEL device.

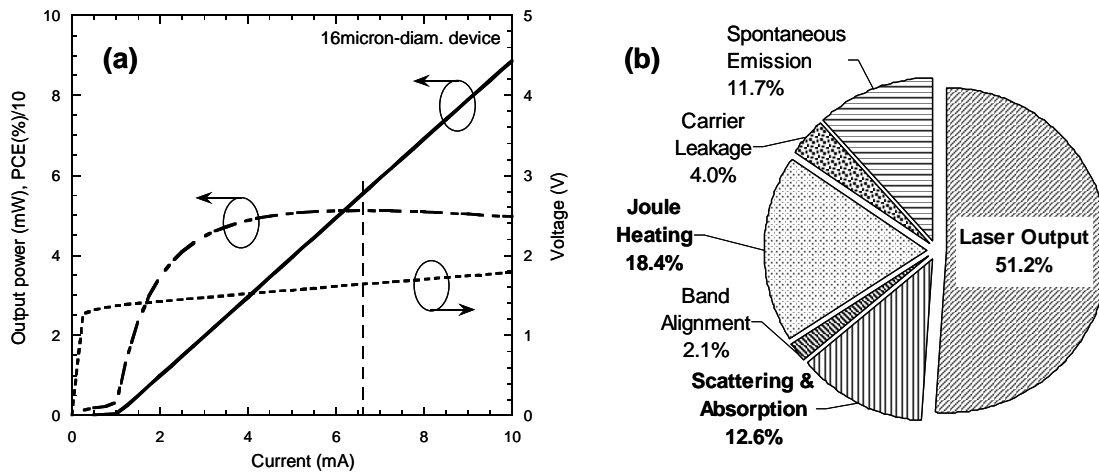


Fig. 2. (a) L-I-V characteristics of a high-efficiency, bottom-emitting, 976nm VCSEL device. The oxide aperture diameter is 16µm. A maximum PCE of 51.2% is achieved. (b) Pie diagram showing the different sources of power consumption in the device operating at maximum PCE.

From a power consumption budget analysis at the maximum PCE operating point, we find that most of the wasted power comes from Joule resistive heating (18.4%) and absorption losses (12.6%). Both account for 31% of the lost power.

To analyze the results, we can extend the work of Bour and Rosen²³ to VCSELs to obtain a simple analytical expression for the maximum PCE of a device as a function of the slope efficiency, threshold current, and resistance:

$$\eta_{e,m} = \eta_d \frac{V_v}{V_0} \left(1 - \frac{2}{1 + \sqrt{1 + \alpha}} \right) \quad (1)$$

where η_d is the differential slope efficiency, V_v is the photon energy voltage (1.27V for 976nm lasers), V_0 is the zero-current intercept of the linear portion of the laser I-V characteristic (also referred to as the “turn-on voltage”), and α is a characteristic device parameter defined as $\alpha = V_0 / (I_{th} R_d) = V_0 / (J_{th} \rho_d)$, where I_{th} (J_{th}) and R_d (ρ_d) are the threshold current (threshold current density) and the resistance (resistivity) of the device considered, respectively. The expression in (1) is obtained by simply assuming that the output power and voltage vary linearly with the current after threshold, and at least up to the point of maximum wall-plug efficiency. This is the case for our VCSELs, as can be seen from Fig. 2. In this case, the device series resistance and differential resistance are the same and referred to simply as the device resistance from now on. The problem of increasing a device’s PCE then reduces to one or all of the following: increasing the slope efficiency, decreasing the resistance, and/or decreasing the threshold current. Reducing V_0 will also help increase the PCE, although the contribution is minor.

Note that for $\alpha \gg 1$, equation (1) approximates to

$$\eta_{e,m} \approx \eta_d \frac{V_v}{V_0} \left(1 - \frac{2}{\sqrt{\alpha}} \right), \quad (2)$$

but in practice, the above relation is useful only for $\alpha > 50$, in which case the error in estimating the maximum wall-plug efficiency of a device is less than 5%. However, $\alpha > 50$ is rarely achieved for VCSELs. For example, for the device in Figure 2, $\alpha = 28$.

To better understand how the different device parameters contribute to device's maximum PCE, we can examine the following relation derived from (1), which expresses the relative change in PCE as a function of the relative changes in slope efficiency and α :

$$\frac{\Delta \eta_{e,m}}{\eta_{e,m}} = \frac{\Delta \eta_d}{\eta_d} + \frac{1}{\sqrt{1+\alpha}} \frac{\Delta \alpha}{\alpha}. \quad (3)$$

Clearly, α contributes significantly less than the slope efficiency to changes in PCE. For example, for a typical value of α of 24, an increase in α will contribute five times less to the increase in PCE than the same relative increase in slope efficiency. Or, put another way, to get the same improvement from a 5% relative increase in slope efficiency (70% to 73.5% for example), the device resistance would need to be decreased by approximately 30%. Therefore, to improve a device's PCE, it is much more critical to first work on increasing the slope efficiency rather than decreasing the threshold current or resistance. A corollary to this observation is that since the slope efficiency is directly proportional to the internal quantum efficiency (see ²⁴ for example), it is also critical to develop a good design and growth process for the multi-quantum-well cavity. We grew top-emitting VCSEL structures with the same cavity design and growth conditions as the bottom-emitting material and extracted an internal quantum efficiency of ~95% by varying the output mirror reflectivity (see ¹⁸ for example).

The α -parameter is a useful metric to quickly evaluate device performance. In practice we found that $\alpha < 10$ corresponds to poor performance (unless the slope efficiency is exceptionally high) and $\alpha > 50$ corresponds to exceptional performance for a VCSEL device (for 976nm devices, with $V_0 \sim 1.33V$). Furthermore, α can be obtained directly from the derivative analysis of the I-V characteristic ^{25,26}, without the need for any optical measurements (the threshold current is determined from the pinning of the junction voltage).

To analyze the device size dependence of the maximum PCE, the size-dependent analytical expressions for the threshold current and slope efficiency derived by Hegblom et al. are used ²¹. These take into account current and carrier spreading, which are a major contributor to loss of performance. These expressions are given by:

$$I_{th} = J_{inf} \pi r_a^2 + \frac{I_0}{2} + r_a \sqrt{\pi I_0} J_{inf} \quad (4)$$

$$\eta_d = \eta_{inf} / (1 + D_0 / D_a) \quad (5)$$

where r_a (D_a) is the device aperture radius (diameter), I_0 is a characteristic spreading current, D_0 is a characteristic spreading distance, and J_{inf} and η_{inf} are the threshold current density and differential slope efficiency without spreading (infinitely large aperture), respectively. The parameters J_{inf} and η_{inf} depend only on the structure intrinsic parameters, such as the mirror reflectivities, the internal loss (that can include such effects as aperture scattering losses for very small devices), the number of quantum wells, the confinement factor, the internal quantum efficiency and material gain parameters. Analytical expressions for J_{inf} and η_{inf} can be found in ²⁴ for example.

For a bottom-emitting structure with the P-DBR as the back reflector, the size-dependent resistance is modeled as the sum of two resistances in parallel:

$$\frac{1}{R_d} = \frac{1}{R_L} + \frac{1}{R_V} = \frac{2\pi r_a}{\rho_0} + \frac{\pi r_a^2}{\rho_{inf}} \quad (6)$$

where ρ_{inf} ($\Omega \cdot \text{cm}^2$) and ρ_0 ($\Omega \cdot \text{cm}$) are characteristic resistivities. The first term R_L accounts for constriction or spreading, lateral and contact resistance (scales inversely with aperture perimeter) while the second R_V term models a uniform

vertical current flow resistance (scales inversely with aperture area). In practice, we found that using this model always fit our simulated and measured data for bottom-emitting devices very well over a wide range of aperture diameters. This model can be compared to that of a top-emitting structure (with the P-DBR as the output mirror), in which the resistance is represented as a series sum of R_L and R_V ²⁷. The two cases are illustrated in Figure 3.

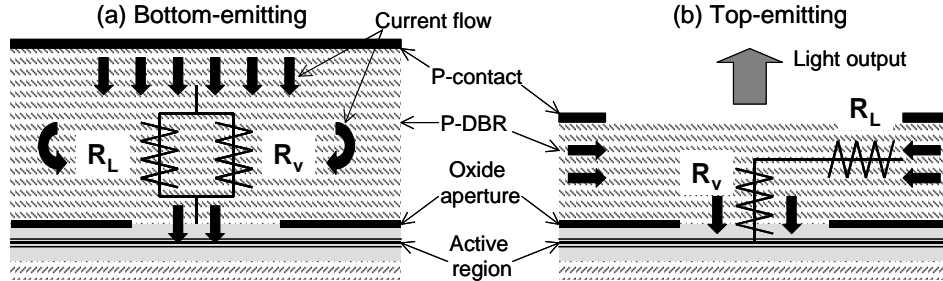


Fig. 3. Schematic representation of the effective resistance network for (a) a bottom-emitting and (b) a top-emitting VCSEL structure.

In the case of the bottom-emitting structure, for infinitely large apertures the resistance will scale as the aperture area, with ρ_{inf} being essentially the vertical resistivity of the P-DBR. This situation has important implications for the scaling of the PCE with device size.

Figure 4 plots the threshold current, the inverse resistance, and the differential slope efficiency as a function of device diameter D_a for high-efficiency bottom-emitting VCSEL devices. Equations (4), (5), and (6) are used to fit the data. The extracted characteristic parameters for this structure are given in Table 1. These seven parameters are sufficient to fully characterize a particular structure in terms of PCE performance.

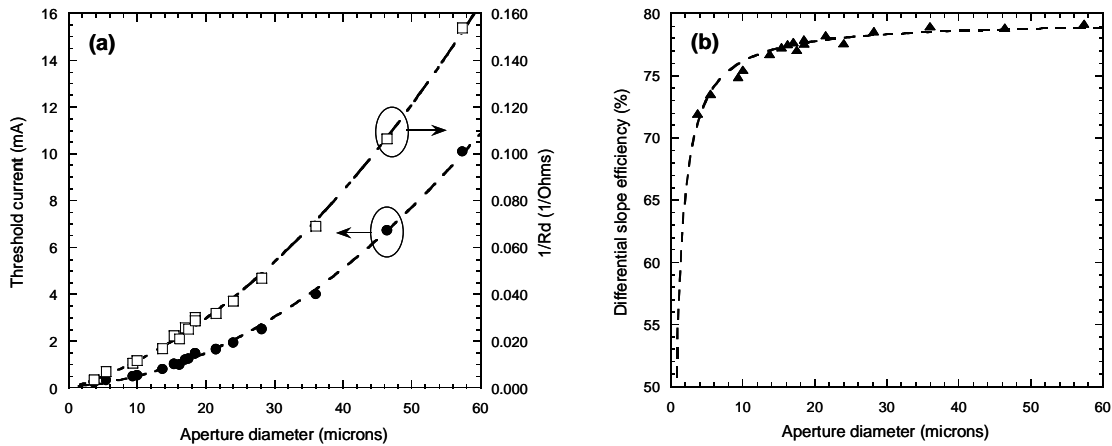


Fig. 4. (a) Threshold current and inverse resistance, and (b) differential slope efficiency as a function of device aperture diameter. The symbols are measured data and the lines represent best fits to using the analytical formulas.

Although in the present work we used the expressions for the threshold current, resistance, and slope efficiency to fit the data, we also use these same expressions to fit simulated results for design optimization. In this case we deduce the parameters of Table 1 from more advanced simulations. For example, we determine the current distribution (and the resulting carrier profile in the active region) from finite element simulations, and we can then extract I_0 , D_0 , ρ_{inf} , and ρ_0 for a particular design. This knowledge helps accelerate the design optimization process.

Table 1. Extracted VCSEL characteristic parameters.

| Description | Symbol | Value | Unit |
|--|--------------|---------|--------------------------|
| Turn-on voltage (zero-current intercept) | V_0 | 1.33 | V |
| Threshold current density (infinite aperture size) | J_{inf} | 343.6 | A/cm ² |
| Characteristic spreading current | I_0 | 0.126 | mA |
| Vertical resistivity | ρ_{inf} | 2.52e-4 | $\Omega\cdot\text{cm}^2$ |
| Lateral resistivity | ρ_0 | 0.363 | $\Omega\cdot\text{cm}$ |
| Characteristic spreading diameter | D_0 | 0.431 | μm |
| Slope efficiency (infinite aperture size) | η_{inf} | 79.5 | % |

Using these extracted parameters and the measured value $V_0=1.33\text{V}$ (roughly independent of device size), α and $\eta_{e,m}$ (maximum PCE) are plotted against the measured data (Fig. 5).

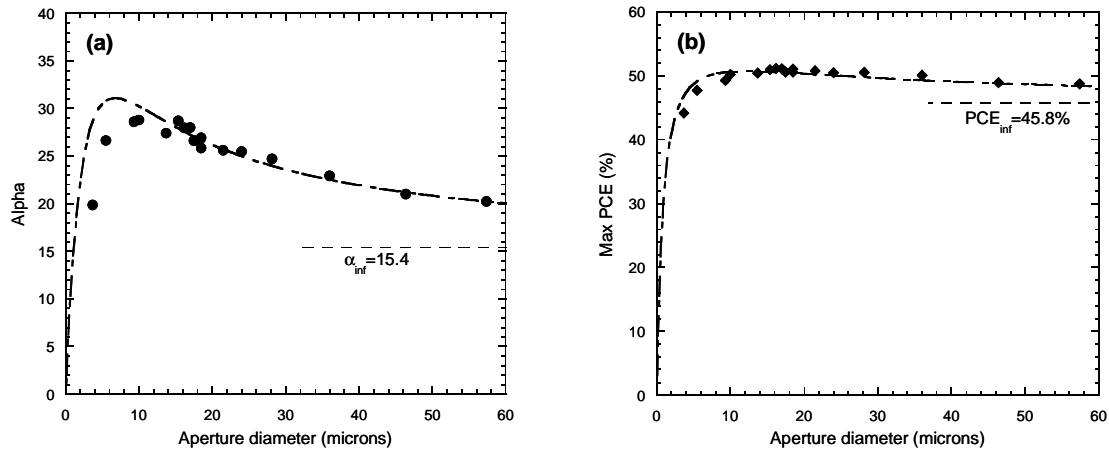


Fig. 5. (a) α -parameter and (b) maximum PCE as a function of device aperture diameter. The symbols are data and the lines were obtained using the analytical expressions and the parameters extracted in Table 1.

As can be seen in this case, α and $\eta_{e,m}$ have optimal values. The PCE characteristic is relatively flat over a wide range of device diameters, exceeding 50% in the range 10~30 μm (data). More interestingly, α and $\eta_{e,m}$ converge towards constant values for infinitely large aperture diameters. These values are given by

$$\alpha_{inf} = \frac{V_0}{J_{inf} \rho_{inf}} \quad (7)$$

$$\eta_{e,inf} = \eta_{inf} \frac{V_v}{V_0} \left(1 - \frac{2}{1 + \sqrt{1 + \alpha_{inf}}} \right). \quad (8)$$

For the devices studied in this work, using the values in Table 1, we obtain $\alpha_{inf} \sim 15.4$ and $\eta_{e,inf} \sim 45.8\%$. This result means that for a bottom-emitting geometry, a large aperture size is not necessarily a hindrance to achieving reasonably large PCE. We also note that decreasing J_{inf} and the P-DBR vertical resistivity, and increasing η_{inf} are a good place to start to maximize device efficiency.

It can be shown that the existence of a local maximum for the parameter α depends only on a dimensionless quantity defined as

$$\alpha_0 = 2 \frac{\rho_{\text{inf}}}{\rho_0} \sqrt{\frac{\pi I_{\text{inf}}}{I_0}}. \quad (9)$$

When $\alpha_0 \leq 1$, no local maximum exists for α . Instead, α_{inf} is an absolute maximum, attained for infinitely large aperture diameters. On the other hand, when $\alpha_0 > 1$, a local maximum exists for α . It is always larger than α_{inf} and is given by:

$$\alpha_{\text{opt}} = \alpha_{\text{inf}} \left(1 + \frac{1}{2} \frac{(\sqrt{2\alpha_0(\alpha_0 - 1) + 1} - 1)^2}{\sqrt{2\alpha_0(\alpha_0 - 1) + 1} - 1 + \alpha_0} \right). \quad (10)$$

Note that for $\alpha_0 \gg 1$, the above expression simplifies to

$$\alpha_{\text{opt}} = \alpha_{\text{inf}} \frac{\alpha_0}{1 + \sqrt{2}} \approx 1.47 \frac{V_0}{\rho_0 \sqrt{I_0} J_{\text{inf}}}. \quad (11)$$

Finally, in the case $\alpha_0 > 1$ the expression for the aperture diameter at optimal α is:

$$D_\alpha = \frac{4\rho_{\text{inf}} / \rho_0}{\sqrt{2\alpha_0(\alpha_0 - 1) + 1} - 1} \approx 0.8 \sqrt{I_0 / J_{\text{inf}}} \quad \text{for } \alpha_0 \gg 1. \quad (12)$$

Table 2 summarizes the values for these derived parameters.

Table 2. Derived characteristic parameters and comparison to some measured values.

| Description | Symbol | Derived value | Measured value | Unit |
|--|-----------------------|---------------|----------------|---------------|
| α -parameter for infinitely large devices | α_{inf} | 15.4 | – | – |
| Max PCE for infinitely large devices | $\eta_{e,\text{inf}}$ | 45.8 | – | % |
| Characteristic parameter for determining α_{opt} | α_0 | 4.1 | – | – |
| Optimal α (maximum) | α_{opt} | 31.1 | 29.5 | – |
| Device diameter at α_{opt} | D_α | 6.8 | ~11.5 | μm |
| Optimal PCE (maximum) | $\eta_{e,\text{opt}}$ | 50.7 | 51.2 | % |
| Device diameter at $\eta_{e,\text{opt}}$ | D_η | 12.4 | ~16 | μm |

The derived and measured values for the optimal α and PCE are in good agreement. It is interesting to note that for all devices larger than a certain diameter, the maximum PCE will lie in a relatively narrow range between $\eta_{e,\text{inf}}$ and $\eta_{e,\text{opt}}$ (between 45.8% and ~51% for the devices studied in this work).

Overall, we found that the main obstacle to achieving high efficiency in VCSELs is lateral carrier diffusion in the active region. Current spreading can be virtually eliminated by placing the oxide aperture very close to the quantum wells and/or by proper design of the layer(s) between the aperture and the quantum wells²¹. Optical losses from the oxide aperture are mainly a concern for very small devices (<5micron diameter) and can be virtually eliminated by proper design and placement of the aperture^{19,20}.

The problem is that lateral carrier diffusion still has a significant impact on device performance even for large devices and vanishes very slowly with increasing aperture size: from (4) we can see that the excess threshold current density decreases only as $1/D_a$ in the limit of very large apertures. For example, for a 20micron-diameter device, the

lateral carrier diffusion still accounts for approximately 30% of the total threshold current. Moreover, it also decreases the slope efficiency.

The lateral carrier confinement issue in VCSELs can potentially be addressed by various quantum well interdiffusion techniques²⁸. Recent work using selective quantum-well intermixing²⁹ has demonstrated promising results for VCSELs.

Another approach involves the use of quantum dots (QD)³⁰, which have minimal lateral carrier diffusion. In addition, QD have very low transparency current density ($<20\text{A}/\text{cm}^2$)^{30,31}. Since J_{inf} is directly proportional to the transparency current density, this design could greatly improve the PCE of VCSELs. However, QD can suffer from low internal quantum efficiency, possibly due to non-optimized growth conditions³².

Using the parameters extracted in Table 1 as a starting point, we simulated the PCE assuming no lateral carrier diffusion (LCD) by setting $I_0=D_0=0$. We also simulated the PCE for ideal quantum-dot (QD) VCSELs, with a $20\text{A}/\text{cm}^2$ transparency current density (corresponding to $J_{inf}\sim 115\text{A}/\text{cm}^2$) and an internal quantum efficiency of 95% (we also assumed that for the QD case there was no LCD). These cases are illustrated in Figure 6 for device diameters $>5\text{microns}$ since we did not include small-size loss effects in our simulations. As can be seen, some drastic improvements in PCE can be expected ($>65\%$) for QD-based VCSEL structures.

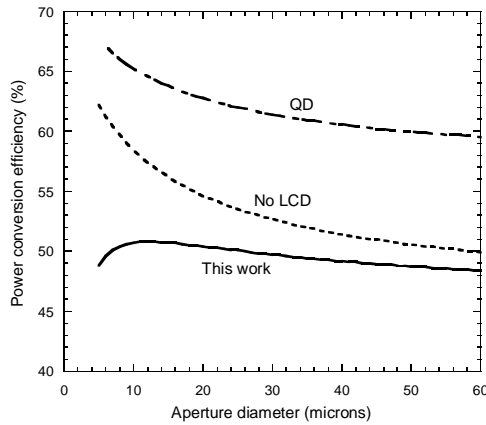


Fig. 6. Plot of the maximum PCE as a function of device diameter for various cases: for current devices (“This work”), assuming no lateral carrier diffusion (“No LCD”), and assuming a quantum-dot-based structure (“QD”).

3. 2D VCSEL ARRAY FABRICATION AND RESULTS

Processing of 2D VCSEL arrays is similar to that of single devices. A cross-section schematic of the processed sample is shown in Figure 7. There are a few more processing steps such as plating of the N- and P-contacts for uniform current distribution within the array.

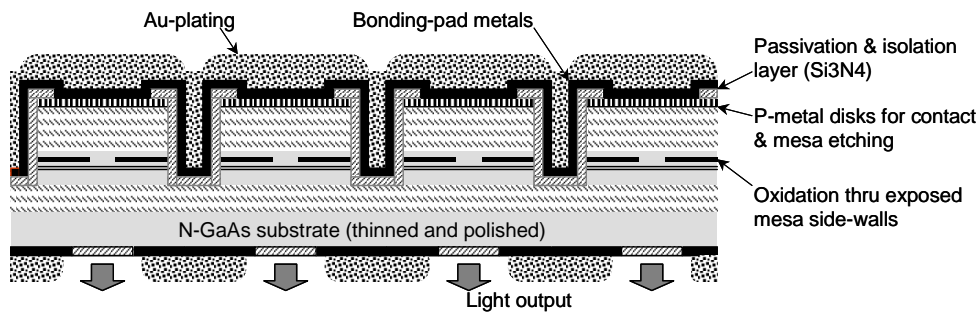


Fig. 7. Schematic cross-section of a 2D VCSEL array.

We found that our selective oxidation process was extremely uniform within an array and from array to array within the same sample. Thus, we believe the selective oxidation process is well suited for VCSEL arrays even larger than 5mm x 5mm and for the production of these arrays.

These arrays are tested at the wafer level (before cleaving and separation) to check for performance and excessive “dead pixels” for example. After cleaving and sorting, individual arrays are soldered onto metallized high-thermal-conductivity submounts such as diamond or BeO. For packaging on diamond submounts, the plating thickness is optimized and an appropriate solder is chosen to account for the large CTE mismatch with GaAs. Then, the chip-on-submount can be packaged onto a micro-channel cooler to increase the heat removal capacity, especially for CW operation.

For properly designed arrays, there is little drop in PCE compared to the single device results. Figure 8 shows a ~5mm x 5mm VCSEL array chip fully packaged on a micro-channel cooler and the LIV characteristics of a high-efficiency array. This array achieves a maximum PCE of 51% (similar to a single device) at a CW output power of 13W.

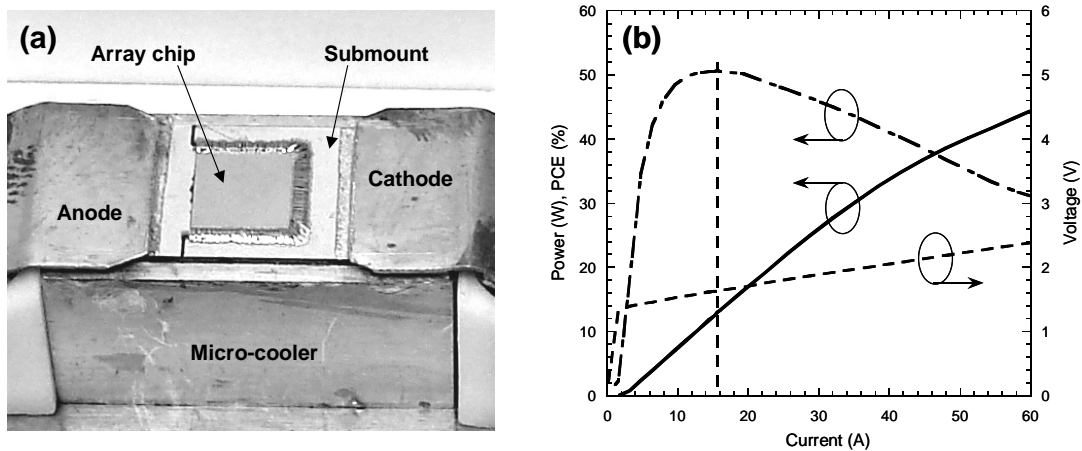


Fig. 8. (a) Picture of a fully packaged 2D VCSEL array on micro-cooler and (b) CW LIV characteristics. The array achieves a maximum PCE of 51% for an output power of 13W at 16A.

For higher power and power density, arrays with more closely spaced elements were fabricated for CW and quasi-CW (QCW – typically 1~500μsec pulse-width and 0.1~10% duty-cycle regime) operation. Care must be taken to avoid thermal crosstalk effects^{33,34}. The results are shown in Figure 9.

The CW array has an emission area of ~0.22cm² and was operated under constant heat-sink temperature (15°C). A record 231W output power was reached at a 320A drive current, limited by thermal roll-over, corresponding to a power density of 1kW/cm². This array has a peak conversion efficiency >44%.

The QCW chip is smaller (0.028cm² area) and was designed to operate in the 100~125A window. The chip-on-submount was not packaged on a micro-channel-cooler. Instead, it was tested directly on a TEC-controlled stage maintained at 20°C. A QCW power of 100W is achieved at 125A, corresponding to a record 3.5kW/cm² power density.

The wavelength spectrum and intensity far-field profile were measured at 100W (~125A) for the 230W array and the results are shown in Figure 10. The beam is circular, with a quasi-top-hat profile. The 1/e² full-width divergence angle is 17°. Since such beam characteristics can be achieved without any optics, VCSEL arrays present a cost-effective solution for direct end-pumping applications.

The spectral full-width half-maximum (FWHM) is only 0.8nm, about five times less than the spectral width of edge-emitter bars or stacks (typically in the 3 to 5nm range). We also measured the wavelength shift as a function of the heat-sink temperature to be 0.065nm/K, identical to the value for single devices. This value is five times less than that of

edge-emitters (typically 0.33nm/K). Therefore, similarly to single-devices, high-power VCSEL arrays benefit from an intrinsic narrow spectrum and stable emission wavelength. This is useful for many pumping applications where the medium has a narrow absorption band.

Our current 3" production wafers have a Fabry-Pérot etalon-wavelength standard deviation of less than 1nm. Such excellent uniformity was achieved through optimization of the growth process for these particular VCSEL structures. From thermal simulations, we expect that the spectral width will not increase significantly for larger size (cm) chips.

Initial reliability results (a few thousands hours) show very little degradation for these arrays, in agreement with previous work ⁶ in which the authors reported more than 10,000 operating hours for a smaller 1W array.

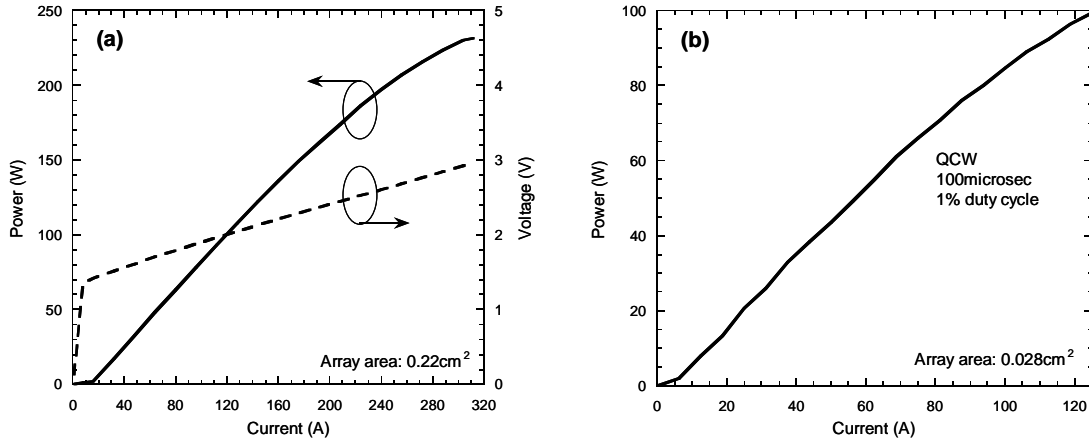


Fig. 9. (a) High-power VCSEL array achieving 231W of CW output power at 320A. (b) High-power density QCW VCSEL array. At 125A, the output power is 100W, corresponding to a 3.5kW/cm² power density.

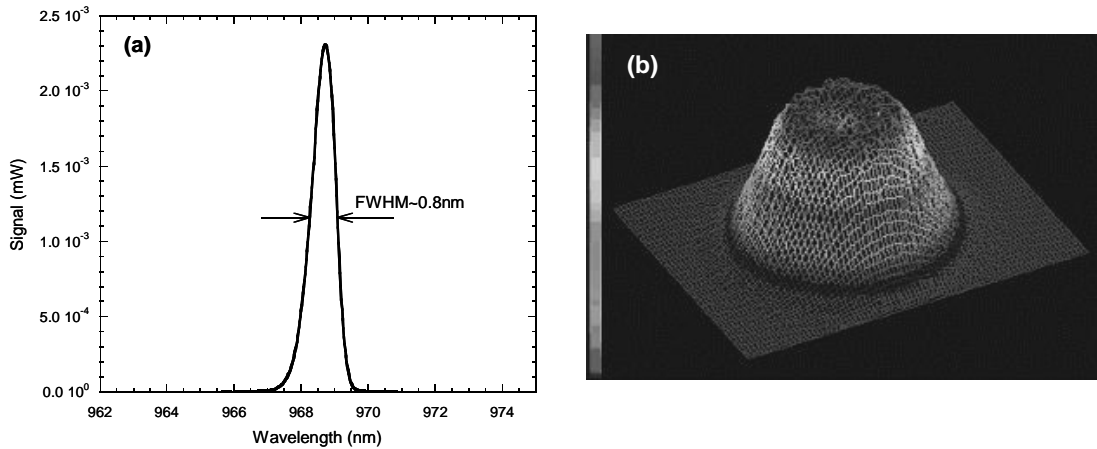


Fig. 10. (a) Wavelength spectrum and (b) far-field intensity distribution at a 100W output power (~125A) from the 231W array shown in Fig. 9(a).

4. HIGH-BRIGHTNESS VCSEL ARRAYS

Certain applications, such as fiber lasers, require that the pump light be fiber-coupled. In this case, a high brightness source is required. In the case of VCSELs, a high-brightness 2D array can be fabricated using thousands of small devices operating in single-mode (the theory behind this approach will be presented elsewhere). Then, by using a micro-lens array with the same footprint as the VCSEL array, the output power from the array can be efficiently coupled into a fiber using a simple focusing lens (Fig. 11).

For this purpose, we have developed small, high-efficiency single-mode devices. Typical LIV and spectral characteristics are shown in Figure 12.

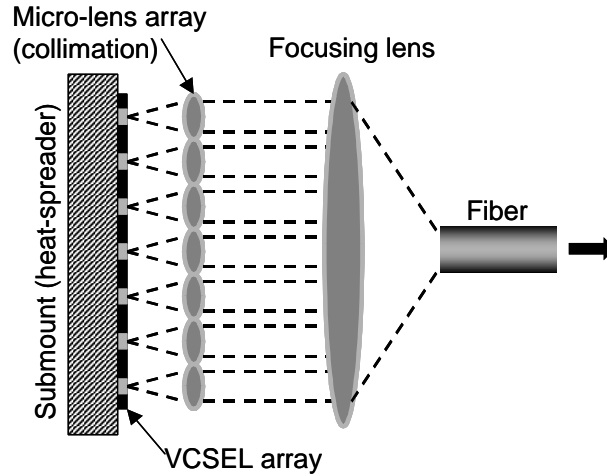


Fig. 11. Schematic of the high-brightness VCSEL array fiber-coupling scheme.

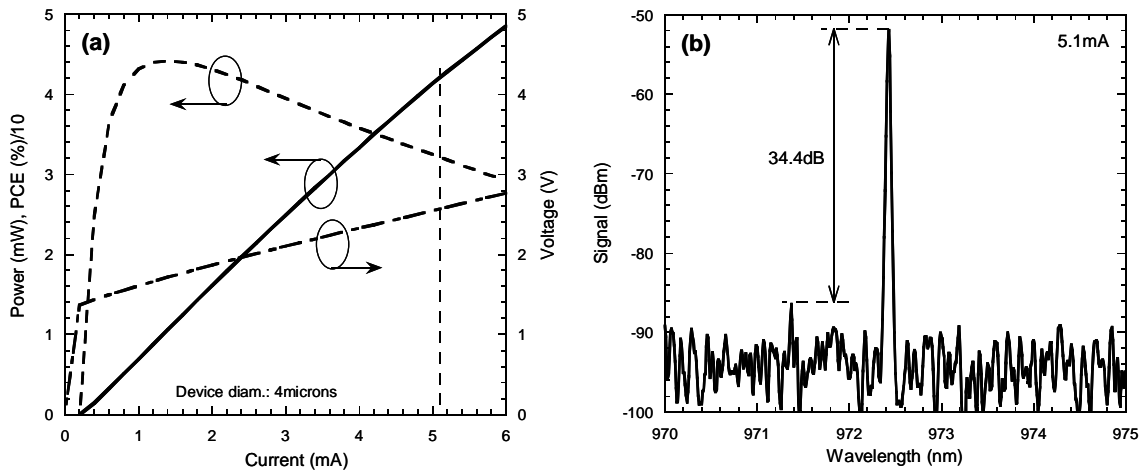


Fig. 12. (a) LIV characteristics of a single-mode VCSEL device. The device operates single-mode up to 4.2mW (5.1mA). (b) Wavelength spectrum at 5.1mA showing a >34dB SMSR.

These devices have a maximum PCE of 44% at 1.1mW output power (single-mode). The maximum single-mode power is 4.2mW at 5.1mA (32% PCE).

Fiber-coupled pump modules were built at 976nm for fiber-laser pumping applications. Figure 13 shows a completed module and the corresponding fiber-out power versus current characteristic. The fiber used has a 400 μ m-diameter core and a 0.46 numerical aperture (NA). Maximum fiber-out power is 40W. Such high-power modules are useful for fiber-lasers because they avoid the need of multiple lower-power edge-emitter pump modules. Furthermore, these modules are intrinsically wavelength-stabilized.

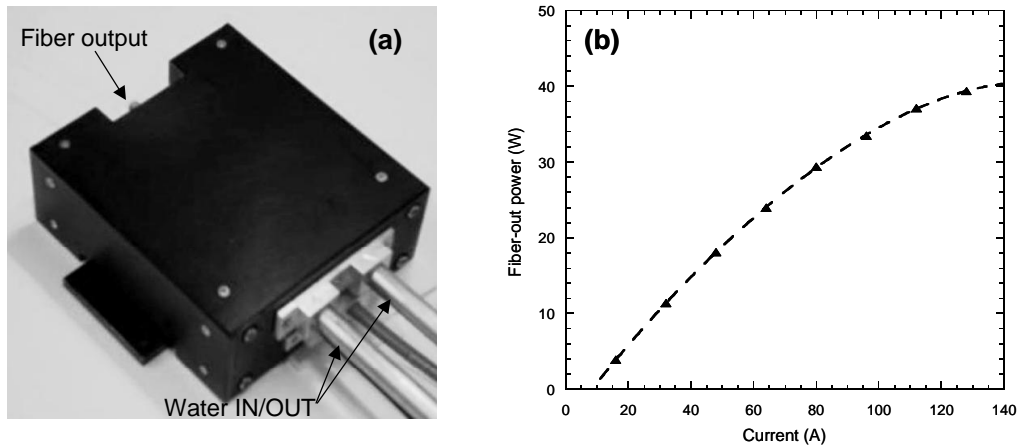


Fig. 13. (a) Picture of the completed high-brightness fiber-coupled VCSEL pump module. The fiber has a 400 μ m-diameter core and a 0.46 numerical aperture. (b) Fiber-out power characteristics.

5. CONCLUSIONS

We have shown that it is possible to use VCSEL technology to make compact high-efficiency high-power pump sources. Bottom-emitting VCSEL devices emitting at 976nm and with power conversion efficiency $>50\%$ were developed. The scaling behavior of these devices showed that even very large aperture devices maintain relatively high PCE. Using these devices, large 2D arrays were fabricated and record CW (230W) and QCW (100W) power levels were demonstrated.

It was also shown that many of the advantages on which low-power single VCSEL devices built their success are preserved for these high-power VCSEL arrays. These advantages include low manufacturing costs, spectral stability and beam quality. Although the conversion efficiency of VCSELs has improved significantly in recent years ($\sim 51\%$), it still lags a bit behind that of edge-emitters ($\sim 60\%$ for commercial products). Still, since VCSELs can operate reliably at high temperature, the overall system efficiency could be higher using VCSELs since a refrigeration apparatus would not be needed.

High-brightness high-power VCSEL-based modules emitting at 976nm were also fabricated for pumping of fiber lasers. These units deliver 40W out of a 400 μ m/0.46NA fiber.

Because of their significant and unique advantages in terms of costs, reliability, and performance VCSELs could become the next technology of choice for compact and efficient high-power semiconductor laser sources for many applications.

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